CLAIMS

1. A method of detecting an error in a persistent memory segment in which values of at least one data item are stored in temporally consecutively allocated memory locations, each new memory location is added to a first end of a block of the memory segment having first and second ends, and a pointer to each new memory location is added to an old memory location in the block containing a preceding value of the at least one data item, the method being characterised by comprising:

(a) determining the address to which the last-added pointer points;

(b) comparing the determined address with an address range of the memory block including the last new memory location (LUM); and

(c) performing an action if the determined address is outside the address range.

2. A method as claimed in claim 1, characterised in that the steps (a) to (c) are performed each time power is applied to the memory segment.

3. A method as claimed in claim 1, characterised in that

the step (a) comprises determining the addresses to which all of the pointers point and selecting the highest or lowest address.

4. A method as claimed in claim 1, characterised in that the step (c) comprises changing the address of the last-added pointer to the address of the last new memory location.

5. A method as claimed in claim 1, characterised in that each new memory location is added contiguously to the first end of the block.

6. A method as claimed in claim 1, characterised in that each pointer points to a highest or lowest address of the memory location to which it points.

7. A method as claimed in claim 1, characterised in that the memory segment comprises at least part of a flash memory.

8. A method as claimed in claim 1, characterised in that each memory location has space for a single value of the at least one data item.

9. A method as claimed claim 1, characterised in that each

bit of the memory segment is individually switchable only from 1 to 0 and the action is performed when the detected address is greater than the highest address of the address range.

10. A method as claimed in claim 1, characterised in that each bit of the memory segment is individually switchable only from 0 to 1 and the action is performed when the detected address is less than the lowest address of the address range.

11. A method as claimed in claim 1, characterised in that the memory segment contains at least one write counter in which a respective flag is set at the end of each value storing operation and a respective further flag is set at the end of each pointer adding operation, and also characterised in that the steps (a) to (c) are performed only if an odd number of flags and further flags is set.

12. A method as claimed in claim 11, characterised in that the at least one write counter comprises a data item.

13. A method as claimed in claim 1, characterised in that the memory segment contains at least one write counter in which, when storing a series of one or more data item values,

a respective flag is set before the first pointer adding operation in the series and a respective further flag is set after the final pointer adding operation in the series, and also characterised in that the steps (a) to (c) are performed only if an odd number of flags and further flags is set.

14. A program for controlling a computer to perform a method as claimed in claim 1.

15. A computer programmed by a program as claimed in claim 14.

16. A storage medium containing a program as claimed in claim 14.

17. An apparatus comprising a persistent memory segment, a portion which stores values of at least one data item in temporally consecutively allocated memory locations with each new memory location being added to a first end of a block of the memory segment having first and second ends, a portion which adds a pointer pointing to each new memory location to an old memory location in the block containing a preceding value of the at least one data item, and

characterised by a portion which determines the address to which the last-added pointer points, a portion which compares the determined address with an address range of the memory block including the last new memory location (LUM), and a portion which performs an action if the determined address is outside the address range.

18. An apparatus as claimed in claim 17, characterised in that the determining portion, the comparing portion and the performing portion are arranged to be actuated each time power is applied to the apparatus.

19. An apparatus as claimed in claim 17, characterised in that the determining portion is arranged to determine the addresses to which all of the pointers point and to select the highest or lowest address.

20. An apparatus as claimed in claim 17, characterised in that the performing portion is arranged to change the address of the last-added pointer to the address of the last new memory location.

21. An apparatus as claimed in claim 17, characterised in that each new memory location is added contiguously to the

first end of the block.

22. An apparatus as claimed in claim 17, characterised in that each pointer points to a highest or lowest address of the memory location to which it points.

23. An apparatus as claimed in claim 17, characterised in that the memory segment comprises at least part of a flash memory.

24. An apparatus as claimed in claim 17, characterised in that each memory location has space for a single value of the at least one data item.

25. An apparatus as claimed in claim 17, characterised in that each bit of the memory segment is individually switchable only from 1 or 0 and the performing portion is arranged to perform the action when the detected address is greater than the highest address of the address range.

26. An apparatus as claimed in claim 17, characterised in that each bit of the memory segment is individually switchable only from 0 to 1 and the performing portion is arranged to perform the action when the detected address is less than

the lowest address of the address range.

27. An apparatus as claimed in claim 17, characterised by comprising: a portion which sets, in at least one write counter in the memory segment, a respective flag at the start of each value storing operation and a respective further flag at the end of each pointer adding operation; and a portion which assesses whether the number of set flags and further flags is odd, the determining portion, the comparing portion and the performing portion being arranged to be actuable in response to the assessing portion.

28. An apparatus as claimed in claim 27, characterised in that the at least one write counter comprises a data item.

29. An apparatus as claimed in claim 17, characterised by comprising: a portion which sets, in at least one write counter in the memory segment and when storing a series of one or more data item values, a respective flag before the first pointer adding operation in the series and a respective further flag after the final pointer adding operation in the series; and a portion which assesses whether the number of set flags and further flags is odd, the determining portion, the comparing portion and the performing portion being

arranged to be actuable in response to the assessing portion.

30. An apparatus as claimed in claim 17, characterised by comprising a smart card.

31. An apparatus comprising a flash memory segment, means for storing values of at least one data item in temporally consecutively allocated memory locations with each new memory location being added to a first end of a block of the memory segment having first and second ends, means for adding a pointer pointing to each new memory location to an old memory location in the block containing a preceding value of the at least one data item, means for determining the address to which the last-added pointer points, means for comparing the determined address with an address range of the memory block including the last new memory location, and means for performing an action if the determined address is outside the address range.